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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/755,283	01/08/2001	Brian Wyld	50990019US	4661

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EXAMINER	
MANOSKEY, JOSEPH D	

ART UNIT	PAPER NUMBER
2184	9

DATE MAILED: 10/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/755,283	Applicant(s) WYLD, BRIAN	
	Examiner Joseph Manoskey	Art Unit 2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9,10 and 12-17* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "32" has been used to designate both the internal memory and I/O device of machine 3 in Fig. 1. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "4", "33", "60", and "62". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to because in Fig. 1, reference sign "43" points to entire machine but according to specification it should point to the I/O device of that machine. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities: the sections of the specification are not titled. Please see the following paragraph for the arrangement of the specification with the corresponding titles. Appropriate correction is required.

5. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(e) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(f) BRIEF SUMMARY OF THE INVENTION.
(g) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(h) DETAILED DESCRIPTION OF THE INVENTION.
(i) CLAIM OR CLAIMS (commencing on a separate sheet).
(j) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(k) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

> the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 9, 12, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakakura et al., U.S. Patent 5,625,795, in view of Papenberg et al., U.S. Patent 5,379,415.

8. Referring to claim 9, Sakakura discloses a distributed multiprocessor system that has at least two hosts connected over a LAN and each host has internal memory accessed by the processing unit. Sakakura also discloses a distributed shared memory card that is interpreted as an access device that provides transparent access to memory external to the host (See Fig. 1, Fig. 2, and Col. 4, lines 9-27). Sakakura does not teach the access device connected to a fault tolerant external memory, however Sakakura does disclose a need to increase the reliability of the communication path and prevent single-point failures (See Col. 2, lines 32-37). Papenberg discloses a fault tolerant memory (See Fig. 2). It would be obvious to one of ordinary skill in the art at the time of the invention to connect the fault tolerant memory of Papenberg to the access device of Sakakura. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because the fault tolerant memory is more reliable and thus less likely to cause a failure of the communication path by eliminating the chance of a single-point failure at the location of the memory.

9. Referring to claim 12, Sakakura and Papenberg teach all the limitations (See rejection of claim 9) including the access device in a host connected to a bus, and the access time to the external memory takes place in less than one cycle of the bus. Sakakura discloses the distributed shared memory card, which interpreted as the

access device, being attached the distributed shared memory bus for access to memory external to each host (See Fig. 1-3). Sakakura also discloses the all access to the memory occurring all within the same cycle (See Fig. 7 and 8).

10. Referring to claim 13, Sakakura and Papenberg teach all the limitations (See rejection of claim 9) including the access device having a memory-mapped connection to the processing unit and a driver connected to the memory-mapped connection and external memory unit. The distributed shared memory card, interpreted as the access device, is connected to the CPU by the I/O bus and the memory bus (See Sakakura, Fig. 2, and Col. 4, lines 18-27). It is interpreted that the access device is memory-mapped since the CPU accesses it through the memory bus. The distributed shared memory card also contains a distributed shared memory controller, which is interpreted as a driver, that is connected to both the I/O bus and the external memory via the DSM bus (See Sakakura, Fig. 3).

11. Referring to claim 14, Sakakura and Papenberg teach all the limitations (See rejection of claim 9) including the access device having a memory module-like connection connected to the processing unit through a memory bus, and a driver connected to both the internal memory module-like connection and the external memory. The distributed shared memory card, interpreted as the access device, is connected to the CPU by the I/O bus that in turn is connected to the memory bus (See Sakakura, Fig. 2, and Col. 4, lines 18-27). It is interpreted that the access device has a "memory module-like connection" since the CPU must access it through the memory bus. The distributed shared memory card also contains a distributed shared memory

controller, which is interpreted as a driver, that is connected to both the "memory module-like connection" and external memory via the DSM bus (See Sakakura, Fig. 3).

12. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakakura et al. and Papenberg et al. in view of Kobayashi, U.S. Patent 6,125,431.

13. Referring to claim 10, Sakakura and Papenberg teach all the limitations except for the processing unit having an access time to the external memory unit less than three orders of magnitude smaller than the access time to the internal memory unit, however Sakakura does disclose accessing and controlling the memory at a high speed (See Col. 3, lines 9-22). Kobayashi teaches a computer that can adjust the timing and providing an access time to the external memory comparable to that of the internal memory (See Fig. 1-3, and Col. 4, lines 11-28). It would be obvious to one of ordinary skill in the art at the time the invention was made to use the timing control of Kobayashi for accessing the external memory of Sakakura and Papenberg. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows the external memory to be accessed in the same manner as the internal memory (See Kobayashi, Col. 2, lines 17-24).

14. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakakura et al. and Papenberg et al. in view of Stirk et al., U.S. Patent 5,408,627.

15. Referring to claims 15, Sakakura and Papenberg teach all the limitations (See rejection of claim 9) except for the external memory unit containing at least two access service devices connected to the access device of each host, however Sakakura does disclose that multiple hosts are attempting to share a resource that can put a burden on

the system (See Col. 2, lines 25-30). Stirk teaches a configurable multiport memory interface (CMMI) that connects multiple hosts to a memory (See Fig. 1). The CMMI contains port interface logic for each host; this is interpreted as an access server device (See Stirk, Fig. 3A). It would be obvious to one of ordinary skill in the art at the time of the invention to attach the CMMI of Stirk between the distributed system of Sakakura and the fault tolerant memory of Papenberg. This would be obvious to one of ordinary skill in the art at the time of the invention to do because the CMMI provides access to the memory for all the hosts separately so that while one CPU is accessing the memory, others can perform different operations (See Stirk, Col. 2, lines 27-30) and this reduces the burden on the system.

16. Referring to claim 16, Sakakura, Papenberg, and Stirk teach all the limitations (See rejection of claim 15) including the fault tolerant memory comprising a request server connected to the server devices. Stirk discloses the CMMI containing an arbitration state machine and memory interface logic; together these are interpreted as a request server (See Fig. 3B).

17. Referring to claim 17, Sakakura, Papenberg, and Stirk teach all the limitations (See rejection of claim 16) including the fault tolerant memory comprising two memory controllers connected to one or more memory banks (See Fig. 2).

Allowable Subject Matter

18. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 4,780,812 to Freestone et al.

U.S. Patent 6,148,377 to Carter et al.

U.S. Patent 6,295,585 to Gillett, Jr. et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Manoskey whose telephone number is (703) 308-5466. The examiner can normally be reached on Mon.-Fri. (8am to 4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

JDM
October 9, 2003

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
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